ABSTRACT OF THE DISCLOSURE

A method for reordering a scan chain so that the given constraints are met and the peak power dissipation is minimized and disclosed. The constraints include a maximum peak power dissipation, a maximum scan chain length and a maximum distance between two successive registers. The developed tool can be embedded into the existing VLSI design flow for low-power circuit designs. Furthermore, the characteristics are quickly judging if the problem has corresponding feasible solutions and searching the optimal solution. Given the scan chain declaration data and the scan pattern data, the modified ones, which satisfy the constraints, can be obtained.